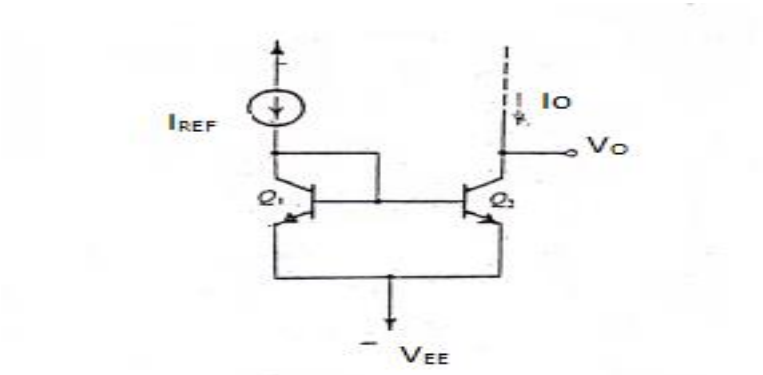
Chapter 1: Op-Amp Circuits

Bias Circuit suitable for IC Design

The bias ckt used to bias discrete BJT are not suitable as they need large no of resistors as well as large coupling and bypass capacitor. With present IC technology it is almost impossible to fabricate large capacitor and it is uneconomical to manufacture large resistance. Biasing in IC design is based on the use of constant current sources. On an IC chip with a number of amplifier stages a constant dc current is generated at one location and is then reproduced at various other locations of biasing the various amplifier stages. This approach has the advantage that the bias currents of the various stage track each other in case of changes in power-supply voltage or in temperature.

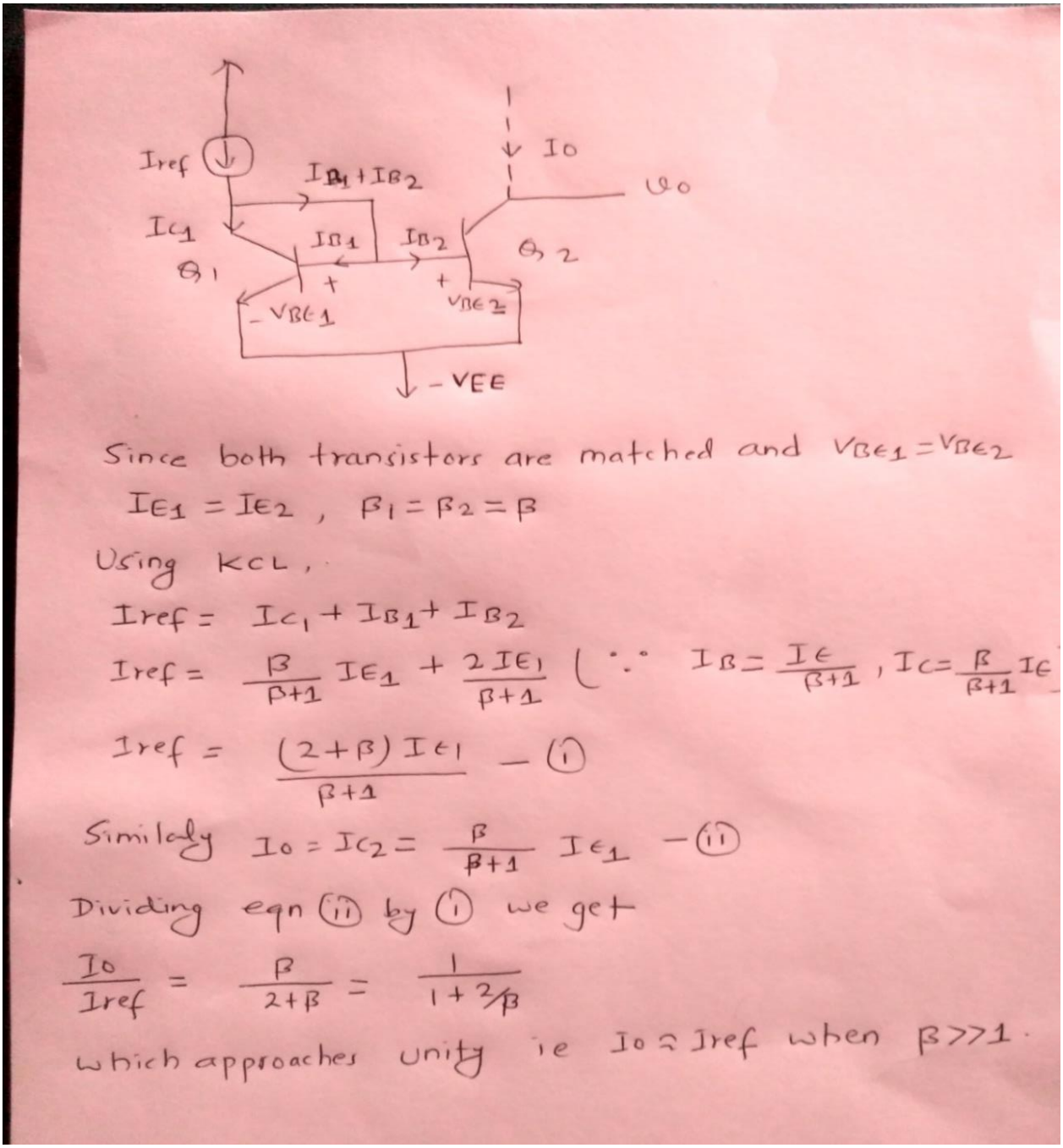
The Current Mirror

The current mirror in its simplest form consists of two matched transistor Q1 and Q2 with their bases and emitters connected together (same V_{BE}).



The basic BJT current mirror

One of the transistors Q1 is connected as diode by shorting its collector to its base. The circuit is fed with a constant current I_{REF} and the out put is taken from the collector of Q2. The circuit fed by the collector of Q2 should ensure active mode operation for Q2 at all times.



Since both transistors are matched and $V_{BE1}=V_{BE2}$

$I_{E1}=I_{E2}$, $\beta_1=\beta_2=\beta$

Using KCL,

$$I_{ref}=I_{C_1}+I_{B_1}+I_{B_2}$$

$$I_{ref}=\frac{\beta}{\beta+1}I_{E_1}+\frac{2I_{E_1}}{\beta+1}\quad\left(\because I_B=\frac{I_E}{\beta+1},\ I_C=\frac{\beta}{\beta+1}I_E\right.$$

$$I_{ref}=\frac{(2+\beta)I_{E1}}{\beta+1}\quad-(i)$$

Similarly $I_o=I_{C2}=\frac{\beta}{\beta+1}I_{E_1}\quad-(ii)$

Dividing eqn (ii) by (i) we get

$$\frac{I_o}{I_{ref}}=\frac{\beta}{2+\beta}=\frac{1}{1+2/\beta}$$

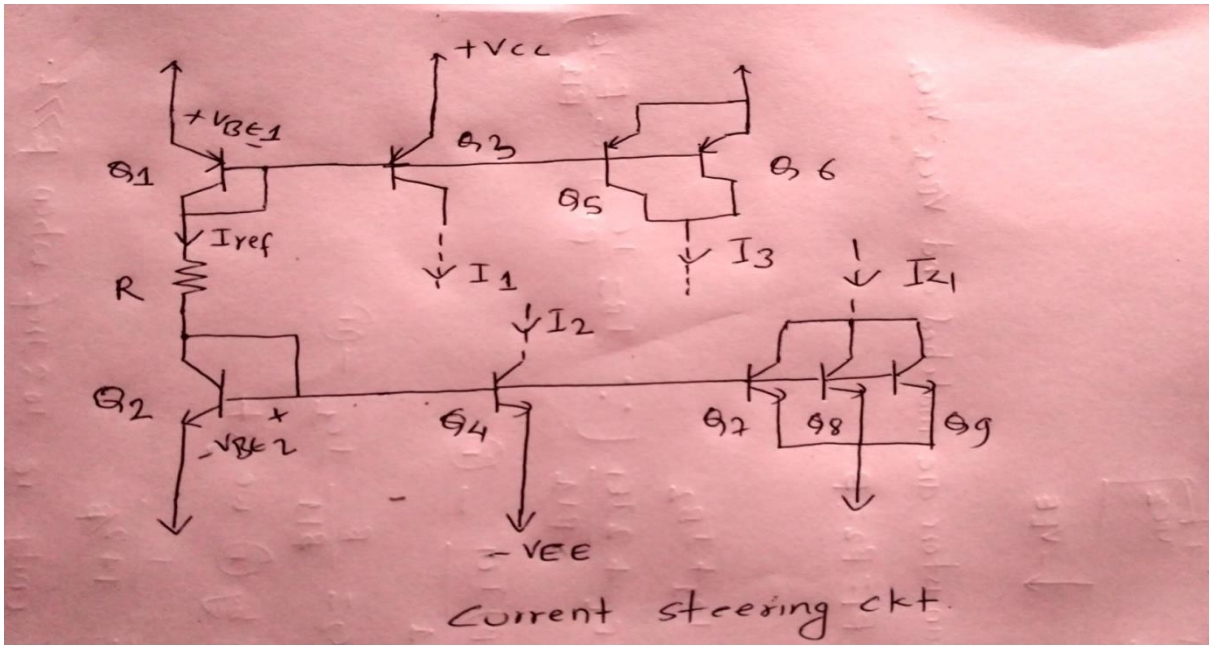
which approaches unity ie $I_o\simeq I_{ref}$ when $\beta>>1$.

But the deviation of current gain from unity can be relatively high β=100 results in 2% error. Another factor that makes Io unequal to Iref is the linear dependence of the collector voltage of Q2 is Io on the collector voltage of Q2. This effect is called early effect. Taking the effect of finite β and early effect together, the output current of the mirror is given by

- $Io=[Iref/(1+2/\beta)][1+V_{CB2}/V_A]$
- Using KVL: $Io=[Iref/(1+2/\beta)][1+(V_0+V_{EE}-V_{BE2})/V_A]$

Steering Circuits

Current mirrors are used in IC fabrication to reproduce current for biasing various ckts.



Diode connected transistors Q1 and Q2 along with resistor R generates a constant dc current Iref.

$$Iref=(V_{CC}+V_{EE}-V_{BE1}-V_{BE2})/R$$

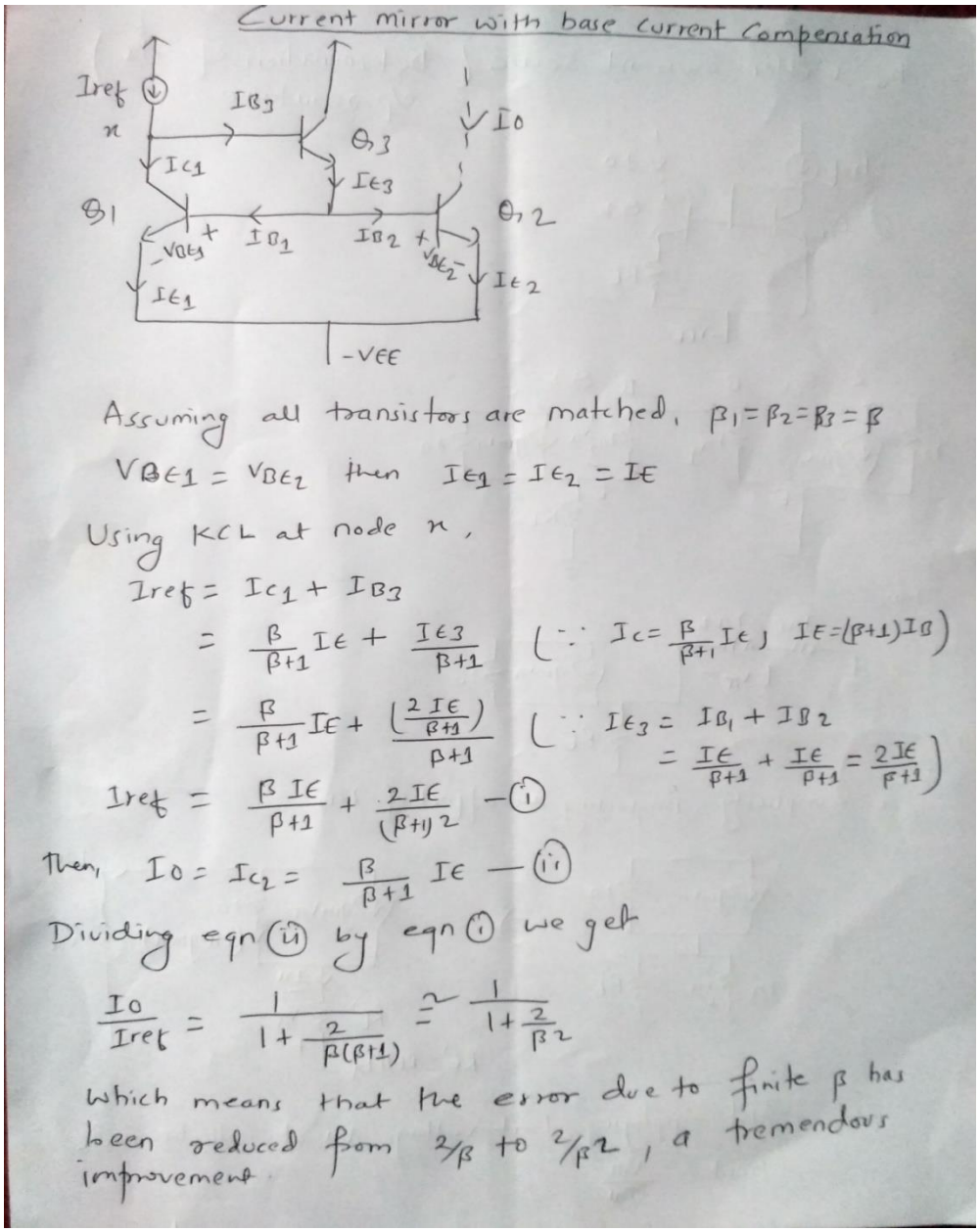
Assuming high β and neglecting early effect, Iref=I1. Q3 can supply this load as long as the Q3 can operate in active region. To generate a dc current twice the value of Iref, 2 transistors Q5 and Q6 are connected in parallel and combination forms a mirror with Q1. Thus I3= 2Iref. Parallel combination of Q5 and Q6 is equivalent to a transistor whose EBJ area is double of Q1. In IC fabrication the EBJ area is doubled if the current has to be doubled. The effect of finite β becomes more severe as the number of o/p of the mirror is increased. This is because the addition of more transistors means that their base current have to be supplied by the reference sources.

Improved Current source

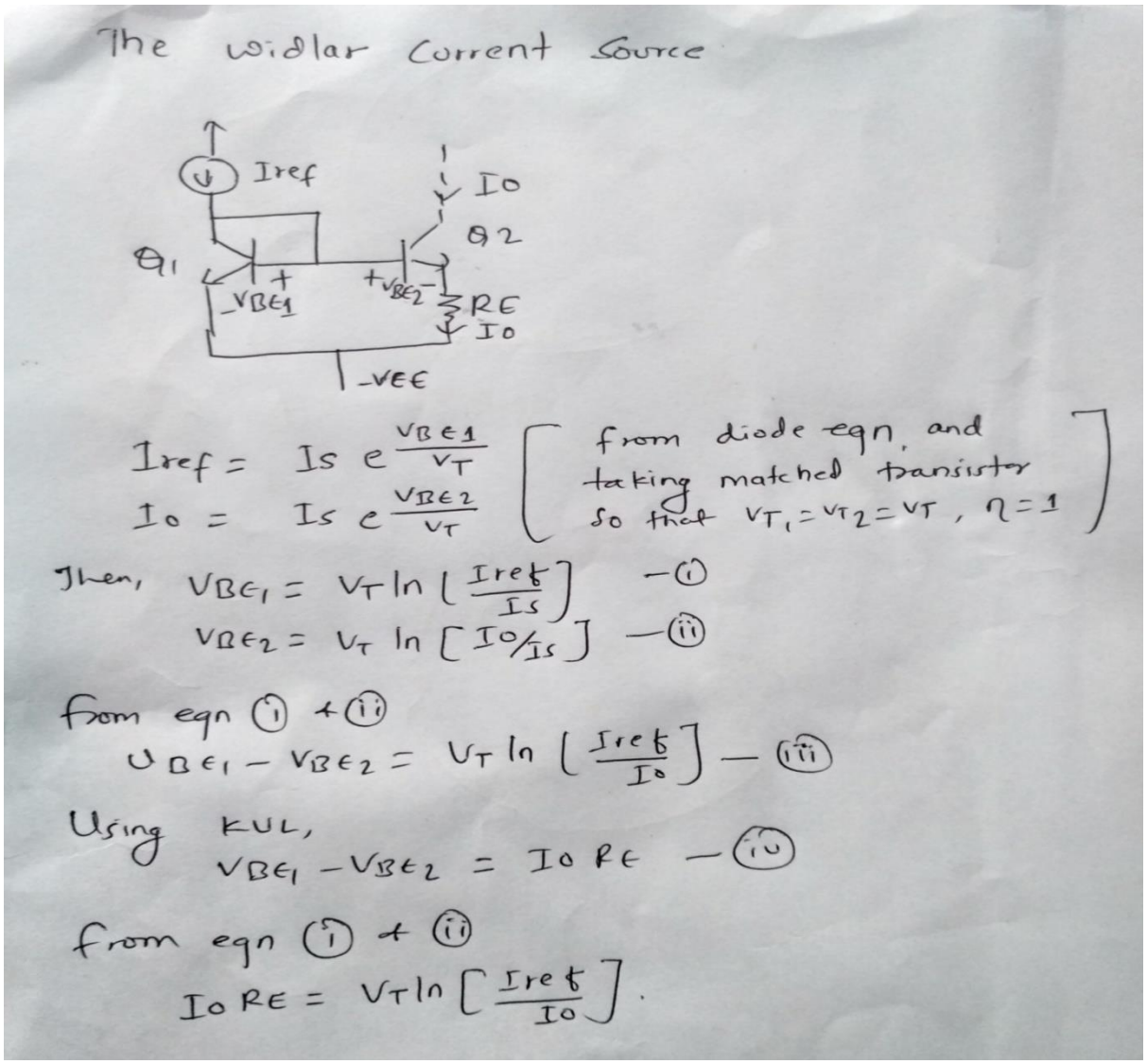
There are two performance parameter of the BJT current source that need improvement

- Dependence of Io on β
- o/p resistance of the current source which was found to be equal to BJT ro, in the order of 100 KΩ. BJT current source are usually used in the place of load resistance Rc of differential amplifier. Thus to obtain high voltage gain, a large o/p resistance is required.

Current mirror with base current compensation

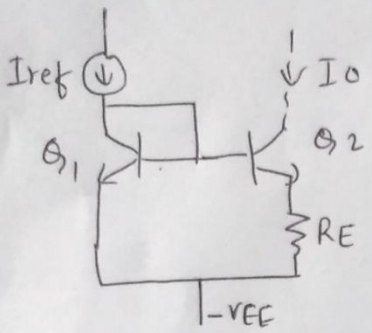


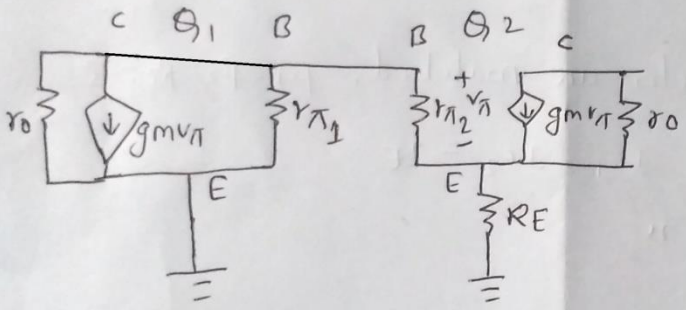
Widlar current source



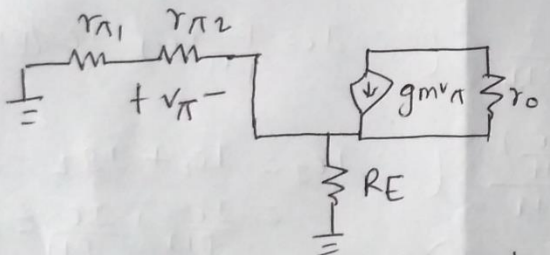
Widlar ckt allows generation of a small constant current using relatively small resistor which results in considerable saving in chip area. Its output resistance is high due to presence of emitter resistance.

The Widlar Current Source (Determination of its o/p resistance)

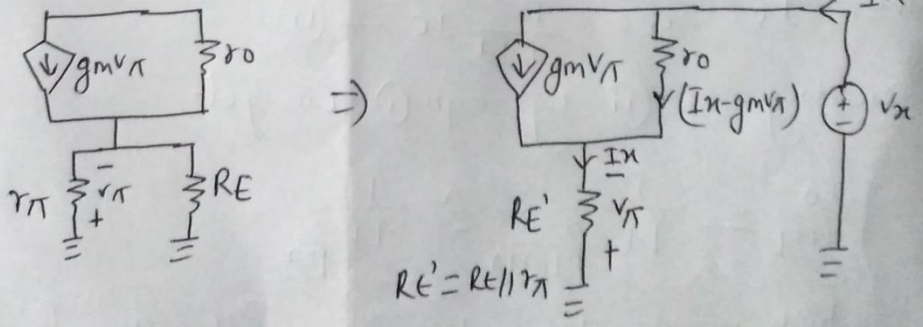




Then,



for simplicity, neglecting the effect of $r_{\pi 1}$



And applying test voltage Vx at collector node

$$R_{out} = \frac{V_x}{I_x}$$

Using KVL,

$V_x = r_o(I_x - g_m V_\pi) + I_x R_E'$

But $V_\pi = -R_E' I_x$

So, $V_x = r_o(I_x + g_m R_E' I_x) + I_x R_E'$

$R_{out} = \frac{V_x}{I_x} = r_o(1 + g_m R_E') + R_E'$

Since $r_o >> R_E'$

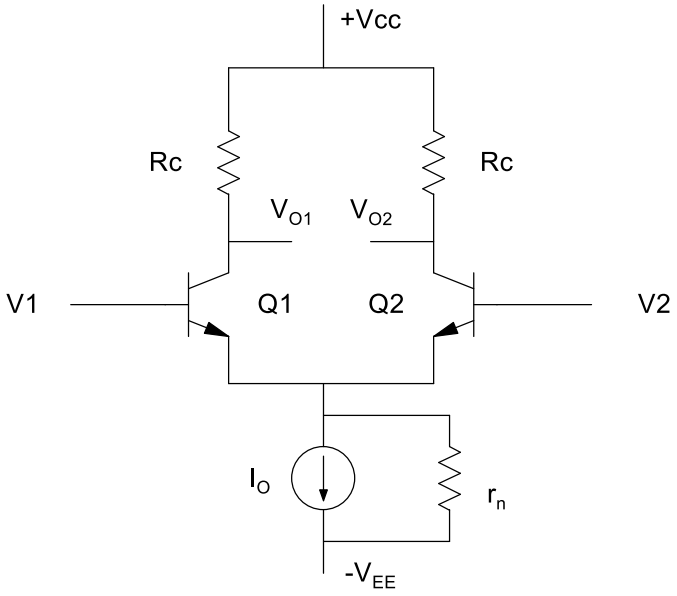
$R_{out} \approx r_o(1 + g_m R_E')$

Thus the o/p resistance is increased by factor $(1 + g_m R_E')$.

Differential Amplifier:

The o/p of differential amplifier is proportional to the difference between two input voltages.

BJT DA



Differential mode response:

Let V_1= Va(t)

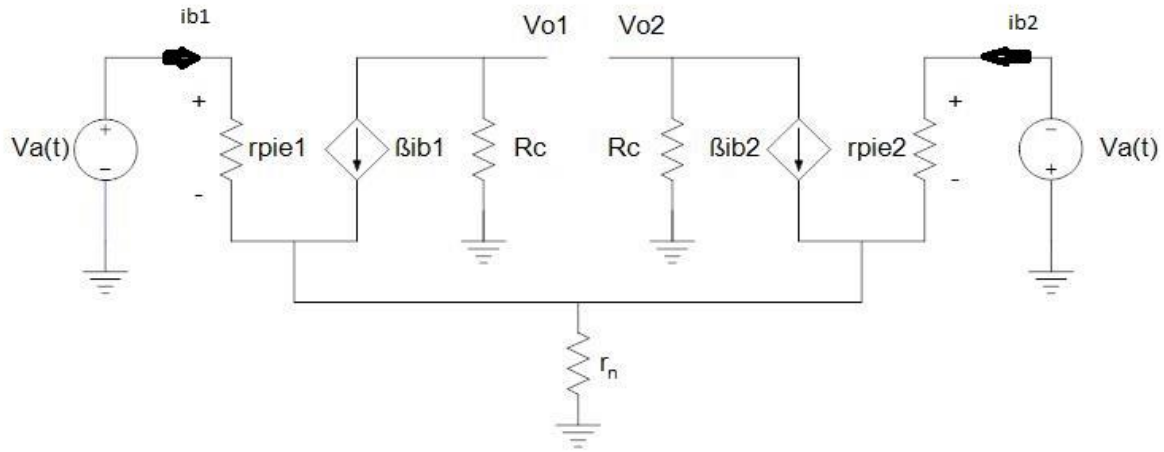
V_2 = -Va(t)

Differential mode input (Vid)= V_1-V_2= 2Va(t)

Common mode input (Vcm)=$\frac{V1+V2}{2}$=0.

It has purely differential mode input signals.

Small signal analysis:



Assuming both transistors are identical and equal dc biasing $\beta 1= \beta 2=\beta$ and $r\pi 1=r\pi 2=r\pi$.

Using KVL, we get

$Va(t)-ib1\ r\pi+ ib2\ r\pi+Va(t)=0$

Form figure, ib1=-ib2, so

$Ib1= \frac{Va(t)}{r\pi}$; $ib2= -\frac{Va(t)}{r\pi}$

Now, output will be

$Vo1=- \beta ib1Rc$

$Vo1=-\frac{\beta Va(t)Rc}{r\pi}$

$Vo2=+\frac{\beta Va(t)Rc}{r\pi}$

Gain of Amplifier:

Differential input single ended output:

$Adiff\text{-}Se1=\frac{Vo1}{Vid} = -\frac{\beta Rc}{2r\pi} = -\frac{gmRc}{2}$

$Adiff\text{-}Se2 = \frac{Vo2}{Vid} = +\frac{\beta Rc}{2r\pi} =+\frac{gmRc}{2}$

Differential input differential output:

$Adiff\text{-}diff =\frac{Vo1-Vo2}{Vid} = -\frac{\beta Rc}{r\pi} = - gmRc$

Common mode response:

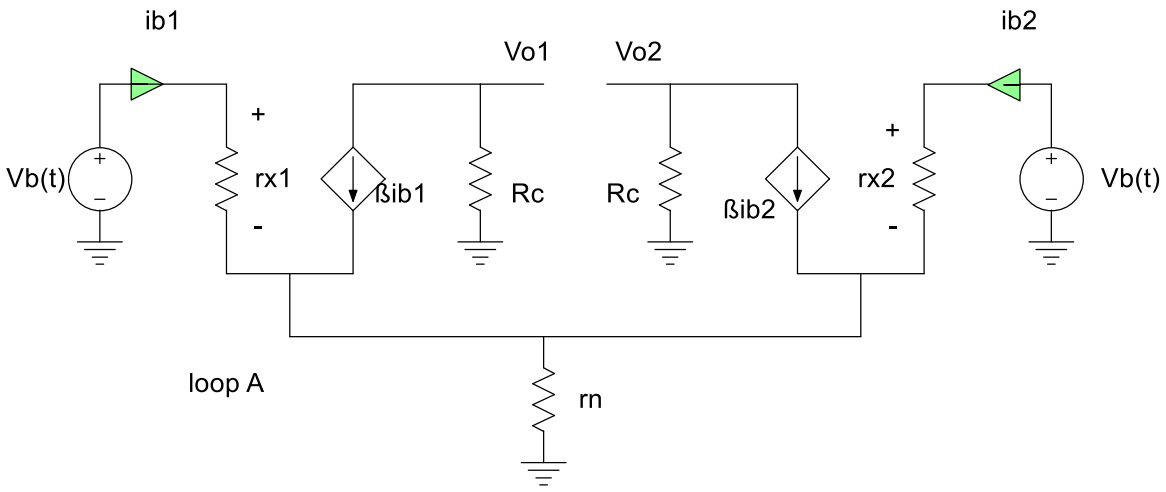
Let $V_1= Vb(t)$

$V_2 = Vb(t)$

Differential mode input (Vid)= V_1-V_2= 0

Common mode input (Vcm)=$\frac{V1+V2}{2}$=Vb(t)

It has purely common mode input signal.



Here rx1=rπ1 and rx2= rπ2. Since both transistors are identical and have equal dc biasing rπ1= rπ2= rπ

And β1= β2= β.

Using KVL at loop A,

Vb(t)= ib1 rπ + 2ib1(β+1)rn

Or, ib1=$\frac{Vb(t)}{2(\beta+1)rn+r\pi}$= ib2

Then, Vo1= -Rcβib1= - $\frac{Vb(t)Rc\beta}{2(\beta+1)rn+r\pi}$; Vo2 = - Rcβib2 = - $\frac{Vb(t)Rc\beta}{2(\beta+1)rn+r\pi}$

Common mode gain;

Acm-Se1= $\frac{Vo1}{Vcm}$ = -$\frac{Rc}{2rn}$ (since rn>> rπ , neglecting rπ and taking β+1≅ β)

Acm-se2= $\frac{Vo2}{Vcm}$ = - $\frac{Rc}{2rn}$

Acm-diff = $\frac{Vo1-Vo2}{Vcm}$ =0

Common mode rejection ratio (CMRR): The term that describes the ability of amplifier to reject common mode signal (noise). Higher the CMRR more it reject the common mode signal.

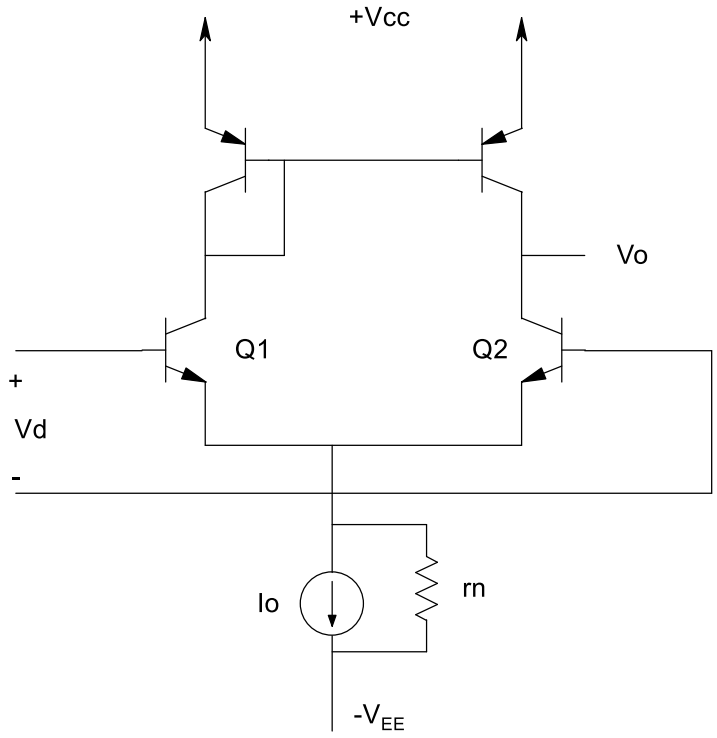
CMRR= $\frac{\text{differential gain}}{\text{common mode gain}}$

In decibel, CMRR= 20 $\log_{10}$ [$\frac{\text{differential gain}}{\text{common mode gain}}$]

Active loads:

Transistors occupy much less silicon area than resistors. So many BJT ICs use BJT loads in place of resistive load Rc. In such circuits, the BJT load is usually connected as a constant current source and thus presents the amplifier transistor with a very high resistance load. So the amplifier that utilizes active load can achieve higher voltage gain than those with passive (resistive) loads.

Differential amplifier with active load:



Voltage gain $=\frac{vo}{vd}=\frac{gmro}{2}$

Substituting $gm=\frac{Ic}{VT}$ and $ro=\frac{VA}{IC}$; $gmro=\frac{VA}{VT}$

Typically VA= 100V, leading to gmro=4000 and a stage voltage gain of about 2000. Without the current mirror the gain would be half the value found above.

Output stage:

The purpose of the output stage is to provide the amplifier with a low output resistance. In addition, the o/p stage should be able to supply relatively large load current without dissipating a large amount of power in the IC.